F I N A L   R E P O R T

Results and Recommendations
Based on Development of a
Prototype Resolver to Digital Encoder
Under NASA Contract Number NAS8-20576

Prepared for

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February 10, 1967

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INTRODUCTION

Our proposal covers in detail the theory of operation of the Resolver to Digital converter proposed for your application. Our basic design approach did not change so the theoretical details will not be repeated.

The design study report discussed effects of resolver TR, phase shift and nulls on converter accuracy and performance. Also included in this report was an updated error table.

The purpose of this report will be to summarize the results obtained on the prototype system and indicate in what areas changes and/or improvements have been made. Pertinent design details will be discussed along with recommendations where applicable.

SUMMARY OF RESULTS

Using the technique described in our June progress report, plots of the analog instrumentation errors were made. These results are shown in figure 1.

The segments of the plot resemble the theoretical linearization error (see page 10 of proposal); but are somewhat masked by a large random error. The random error is caused by the non-ideal characteristics of the electronic components that make up the analog section of the converter. The four main sources of these errors are:

1. Tolerances (± .01%) of precision wire-wound resistors
2. Finite gain of integrated operational amplifiers (infinite gain ideal).
3. Non-ideal switches (FET's)
4. Quadrature

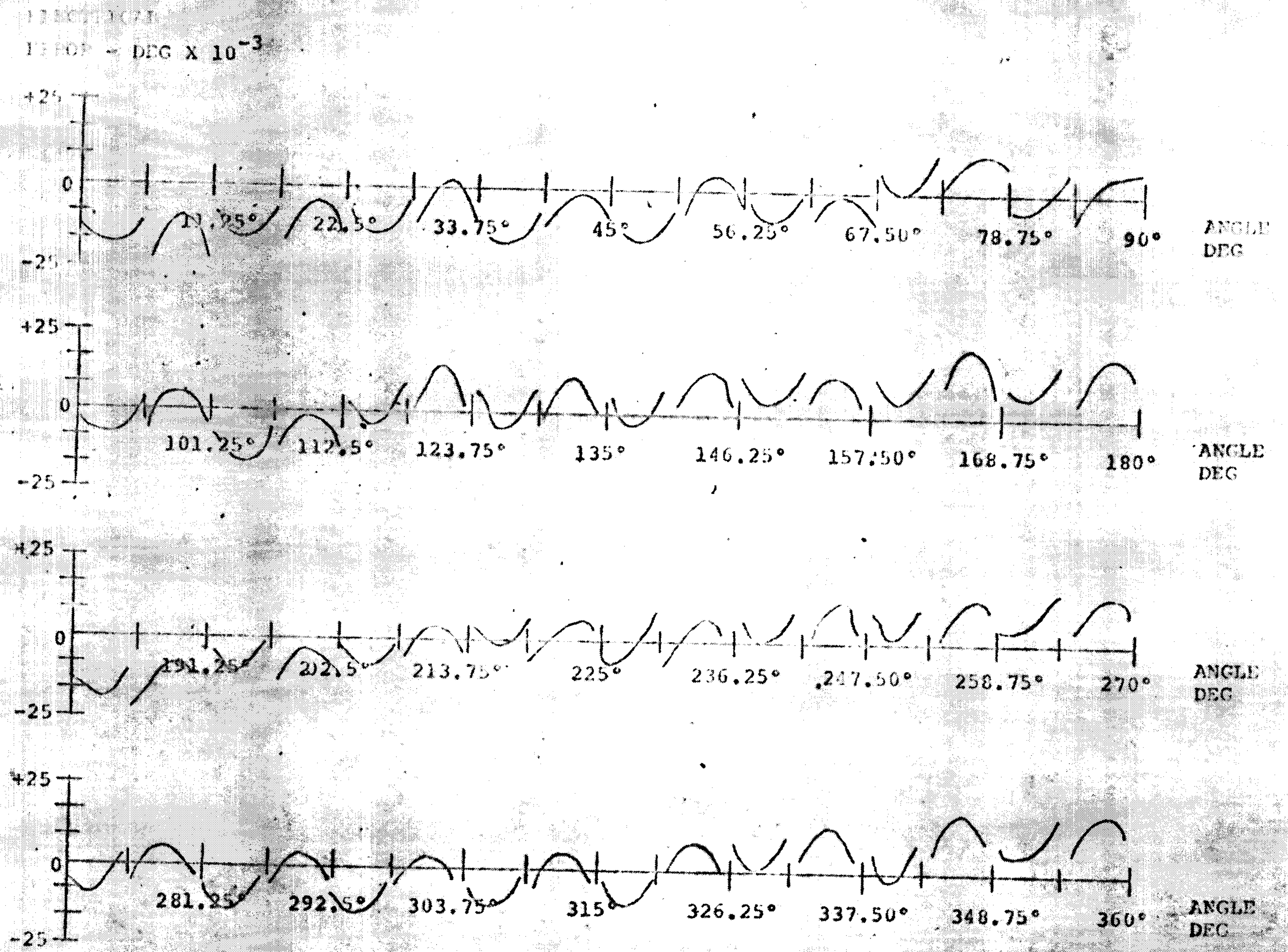

FIG 1 - ANALOG INSTRUMENTATION ERROR

This is the main area where we feel further improvements could be made and will be discussed in more detail in "Recommendations and Conclusions."

A major improvement in system performance was realized by completely eliminating dead zone error. The resulting limit cycle is buffered digitally from the read-out. Also, since resolver TR variations affected the dead zone error, the converter performance is virttally unaffected by resolver parameter variations.

Table 1 shows a summary of predicted and measured errors. Although the peak instrumentation error is considerably higher than predicted, its rms value is reásonable, (1.45 sec RMS).

Final acceptance data was taken using a NASA supplied Bendix 32 and 1 speed resolver. This unit was mounted on an indexing stand and the 32X outputs were monitored on a resolver bridge. The output of the bridge was used to drive a phase angle voltmeter. The resolver outputs were also connected to the encoder. The index stand was set to discrete angles and the resolver outputs were measured on the resolver bridge. This reading divided by 32 is the actual indicated angle thus eliminating resolver and stand inaccuracies. The encoder read-out is then recorded and compared to the bridge reading, the difference being the error at that point.

This technique for final performance subjects the systems to its actual environment. Any errors caused by resolver quadrature or harmonics would be picked up in this test. The results are shown in figure 2 and appear to be in agreement with the results that could be expected from table 1.

ERROR SOURCE	PREDICTED ERRORS (Page 8, Design Study Report)		MEASURED ERRORS	
	Peak (sec)	RMS (sec)	Peak (sec)	RMS (sec)
Instrumentation Error				
Theoretical	±.38	±0.93 (Theoretical)	±0.40	±1.35 (measured)
Random	±.98		±2.10	
Dead Zone	±0.47	±0.16	0	0
Quantization	±1.24	±0.71	±1.24	±0.71
TOTAL ERROR	±3.07 sec Peak	±1.175 sec RMS	±3.74 sec Peak	±1.51 sec RMS

T A B L E I

CONCLUSIONS AND RECOMMENDATIONS

The system delivered under this contract was designed to work with the Bendix type 32 and 1 speed resolver. However, the system can be modified to work with other binary ratioed multi-speed resolvers. This modification would consist of rewiring the coarse system connector and changing the front panel engraving. The present system could be modified by this technique to interface with 8:1, 16:1 and 64:1 speed resolvers. By also adding another counter card multispeed ratios of 128:1 and 256:1 could be handled.

As mentioned earlier, we were a little disappointed in the large random component present in this system. Since this error is caused primarily by the non-ideal characteristics of many of the analog components used in the system, the outlook for further improvement is very promising. Specific areas where improvements could be made are:

1. Precision wirewound resistors. Networks matched to 50PPM and zero TC could be used.
2. FET switches. Many improved switches have been advertised since the design was frozen several months ago.
3. Integrated Operational Amplifiers. This we feel is the most serious error source in the system. However, we are presently and will continue to evaluate new designs. Radiation labs has recently announced a high gain broad band operational amplifier with specifications that appear superior to the Amelco amplifiers used in the present system.

In summary, we feel that the approach is a sound one and the system should give excellent performance. The high usage of integrated circuits will give the system a high degree of reliability. And, if the need should arise, the design could be repackaged for airborne operation. We also feel that the ultimate performance has not been reached but is presently limited by the state of the art of the components used. Since the technology of the components in question is advancing at a very rapid pace, it is felt that this shortcoming will be very quickly eliminated.

INPUT ANGLE (DEGREES) 1X ANGLE	32X ANGLE	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	ACTUAL BINARY ANGLE	OBSERVED	ERROR (MILLIDEGREES)
000.000	45.000	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	359.99931	*	.69
																					000.00000		
																				x	000.00069		
11.602	56.264					x					x										11.60156	*	.49
						x					x									x	11.60225		
34.806	78.792				x	x				x	x									x	34.80538	*	.62
					x	x				x	x								x		34.80606		
45.408	58.056			x							x			x		x			x		45.40793	*	.55
				x							x			x		x			x	x	45.40855		
57.010	69.320			x		x				x				x		x			x		57.00943	*	.20
				x		x				x				x		x			x	x	57.01012		
68.612	80.584			x	x					x	x			x		x			x	x	68.61168	*	.32
				x	x					x	x			x		x		x			68.61237		
80.214	91.848			x	x	x			x					x		x		x			80.21393	*	.62
				x	x	x			x					x		x		x		x	80.21462		
115.022	125.704		x		x				x	x	x			x		x	x				115.02136	*	.05
			x		x				x	x	x			x		x	x			x	115.02205		
126.625	137.000		x		x	x		x						x		x	x		x	x	126.62498	*	.67
			x		x	x		x						x		x	x	x			126.62567		
138.228	148.296		x	x				x			x			x		x	x	x		x	138.22792	*	.61
			x	x				x			x			x		x	x	x	x		138.22861		
149.831	159.592		x	x		x		x		x				x		x	x	x	x	x	149.83086	*	.54
			x	x		x		x		x				x	x						149.83154		
161.434	170.888		x	x	x			x		x	x			x	x					x	161.43379	*	.21
			x	x	x			x		x	x			x	x				x		161.43468		
173.037	182.184		x	x	x	x		x	x					x	x				x	x	173.03673	*	.27
			x	x	x	x		x	x					x	x			x			173.03742		

FIGURE 2 - SHEET 1 OF 2

[illegible]

CONTRACT #[illegible]

ACCURACY DATA

TAKEN BY: [illegible]

DATE: [illegible]

A

B

INPUT ANGLE (DEGREES) 1X ANGLE	32X ANGLE	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	ACTUAL BINARY ANGLE	OBSERVED	ERROR (MILLIDEGREES)
		x			x			x		x		x		x			x		x	x	206.24291		
206.243	164.776	x			x			x		x		x		x			x	x			206.24360	*	.60
		x			x	x		x		x	x	x				x			x		217.80533		
217.806	129.792	x			x	x		x		x	x	x				x			x	x	217.80602	*	.02
		x		x	x			x		x		x				x	x			x	252.61483		
252.615	208.680	x		x	x			x		x		x				x	x		x		252.61551	*	.51
		x		x	x	x		x		x	x	x				x	x		x	x	264.21775	*	.25
264.218	219.976	x		x	x	x		x		x	x	x				x	x	x			264.21844		

FIGURE 2 - SHEET 2 OF 2

R/D CONVERTER

CONTRACT #NAS8-20576

ACCURACY DATA

TAKEN BY: [illegible]

DATE: [illegible]

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